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## **Synopsys Design Compiler Manual - jasonupton.soulsurvivor.nl**

Xilinx Synopsys Interface FPGA User  
Guide — December, 1994 (0401291 01)

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iii Conventions The following conventions are used in this manual's syntactical statements. Courier font System messages or program files appear regular in regular Courier font. Courier font Literal commands that you must enter in ... Design Compiler Design Flow ...

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About This Manual The Design Compiler Command-Line Interface Guide provides basic information about the Design Compiler shell (`dc_shell`), which is the command-line interface to the Synopsys synthesis tools. Audience

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The following documentation is located in the course locker (~cs250/manuals) and provides additional information about Design Compiler, Design Vision, the Design Ware libraries, and the Synopsys 90nm Standard Cell Library.

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- dc-quick-reference.pdf - Design Compiler Quick Reference

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## **IC Compiler II Design Planning User Guide**

An Introduction to the Synopsys Design Compiler Prepared by Li Li for ECE 368 (Instructor: Prof. Shantanu Dutt) 1.

Besides all the source files, we need to write one more file named as "run" (you can name it as you like). In this file,

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these commands are needed:

```
target_library = lsi_10.db symbol_library =  
lsi_10.sdb
```

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12 Design Compiler Interface To use the Synopsys Design Compiler with VHDL Compiler, Design Compiler calls VHDL

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Compiler to translate a VHDL description to a netlist equivalent, then synthesizes that logic into gates in a target technology. The synthesized circuit can then be written back out as a netlist (or other technology-

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## **Design Compiler Command-Line Interface Guide**

4 Manual Design Compiler Build Process  
We will first go through the commands for the tool manually from the commandline so that you can see all the different steps that are required to make the tool work.

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process nodes down to 5nm and beyond.

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2002.05, June 2002 [synqr.book](#) Page i

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